ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

# A CAM CELL BASED CONCURRENT BIST ARCHITECTURE

**V.Lalithamani [*], R.Mythili**

*P.g.scholar, department of electronics and communication engineering,kalaignar karunanidhi institute of technology,coimbatore,india.

Assistant professor, department of electrical and electronics engineering, kalaignar karunanidhi institute of technology,coimbatore,india.

## ABSTRACT

Input vector monitoring concurrent BIST schemes are the class of online BIST techniques that overcomes the problems appearing separately in online and in offline BIST in a very effective way. This paper briefly presents an input vector monitoring concurrent BIST scheme, which monitors a set of vectors called window of vectors reaching the circuit inputs during normal operation, and the use of a CAM memory cell to store the relative locations of the vectors. The proposed scheme is evaluated based on the hardware overhead and the concurrent test latency (CTL) (i.e.)during the normal operation of the circuit, the time required to complete the testing operation; which shows to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff.

**KEYWORDS**: Built-in-Self Test, concurrent testing, input vector monitoring.

## INTRODUCTION

Built-in Self-Test (BIST) techniques constitute an attractive and practical solution to the problem of testing VLSI circuits. BIST eliminates the necessity of high-bandwidth test interactions and allows at-speed testing (time difference between launch and capture event). Other advantages of BIST include reduced product development cycle and cost-effective system maintenance.BIST techniques are typically classified into two types: offline and online. During normal mode, the normal inputs vectors are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV).During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured; therefore, to perform the testing operation, the normal operation is stopped which degrades the system performance.Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation [2]-[10]. These architectures test the CUT concurrently with its normal operation .If the input vector belongs to a set

called active window, the Response Verifier is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in the figure 1. The CUT has n inputs and m outputs and which is tested exhaustively and hence, the test set size is N = 2n.

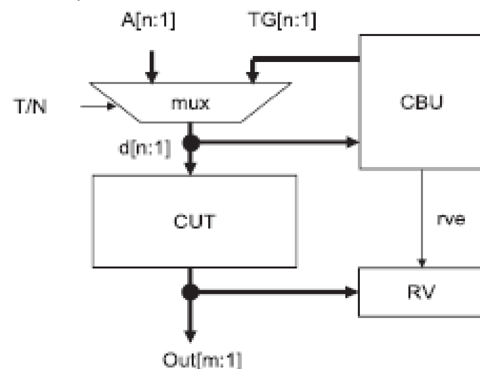


*Fig 1: Input vector monitoring concurrent BIST architecture.*

BIST utilizes a Test Pattern Generator (TG) to generate the test patterns which are applied to the inputs of the Circuit under Test (CUT). Based on signal labeled in the architecture T/N the technique can operate in either normal or test mode.

During normal mode of operation, the CUT inputs are driven from the normal input vector (A[n:1]). A is also driven to the concurrent BIST unit (CBU), where it is compared to a set of active test vectors called window of vectors. If it is found that A matches one of the active windows, we say that the input vector

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

(A) performs a hit. When a hit occurs, A is removed from the active window, and the Response Verifier (RV) captures the CUT response. When all the incoming input vectors have performed a hit, then the content of Response Verifier are examined, to check whether a fault has occurred in the CUT or NOT.

During test mode of operation, inputs to the CUT are driven from the output of Concurrent BIST Unit (CBU) which is denoted by TG [*n*: 1].

In this paper, a novel input vector monitoring concurrent BIST scheme is proposed, which compares the previously proposed schemes [1]–[7] with respect to the hardware overhead and CTL tradeoff. In Section II, the proposed scheme is introduced and in Section III, the simulation results of the proposed one and the comparison results of proposed scheme with existing input vector monitoring concurrent BIST technique are presented. In Section IV the conclusion of this paper is summarized.

## PROPOSED SCHEME

The proposed scheme is to monitor a set of vectors (window), whose window size is W, with W = 2w, where w is an integer number w < n. Let us consider a combinational CUT with n input lines, as shown in Figure 2; hence the possible input vectors for this CUT are 2n.Every moment, the test vectors which belonging to the window are monitored, and the RV is enabled only if the vector performs a hit. The bits of the input vector are separated into two sets consisting of w and k bits, respectively, such that w + k = n. The k (high order) bits of the input vector show that whether the input vector belongs to the window under consideration. The w (lower order) remaining bits shows that the relative location of the incoming vector in the current window. If the input vector that belongs to the current window and has not been received during the examination of the current window, we say that the vector performs a hit and the RV is enabled to capture the CUT's response. After all the vectors that belong to the current window have reached the CUT inputs, the next window is examined.

The module implementing the proposed idea is shown in Figure.2. Depending on the value of the signal *T/N,* it operates one of the two modes. When *T/N* = 0, the module operates in the normal mode. During normal mode, the inputs to the CUT are driven by the normal input vector. The inputs of the CUT are also driven to the Concurrent BIST unit as follows: the *k* (high order) bits are driven to the inputs of a *k*-stage comparator; the w (lower order) bits are driven to the input of the w-stage modified decoder .The other inputs of the comparator are taken from the output of a *k*-stage test generator TG. A logic module based on a Content Addressable Memory (CAM)-like cell, which will be explained shortly.

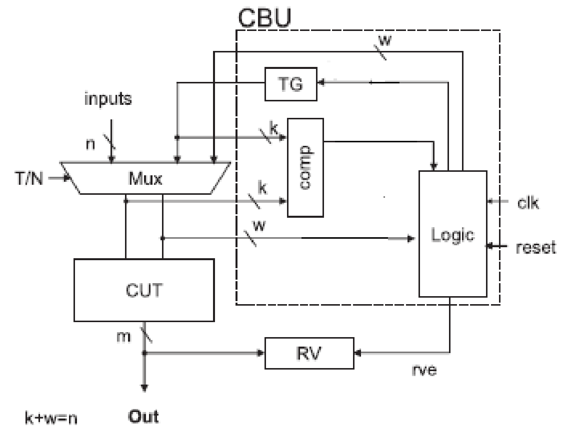


***Fig 2**: Proposed architecture*

The architecture of the proposed scheme for the specific case *n* = 5, *k* = 2, and *w* = 3, is shown in Figure.3.

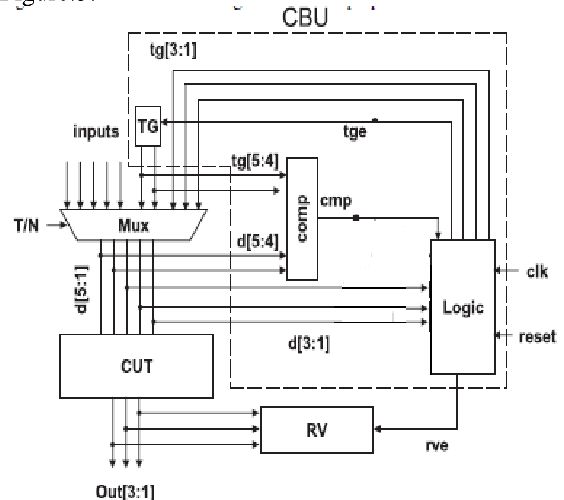


***Fig 3: Proposed architecture for n=5, k=2, w=3.***

***Logic module:***

The logic module of the proposed architecture is shown in Figure.4.It consists of *W* cells and its operation is similar to CAM cell, two *D* flip-flops, and a *w*-stage counter. The overflow signal (ovf) of the counter which drives the tge signal through a unit delay flip-flop. It is assumed that a clock is active during the second half of the operation as shown in the figure.

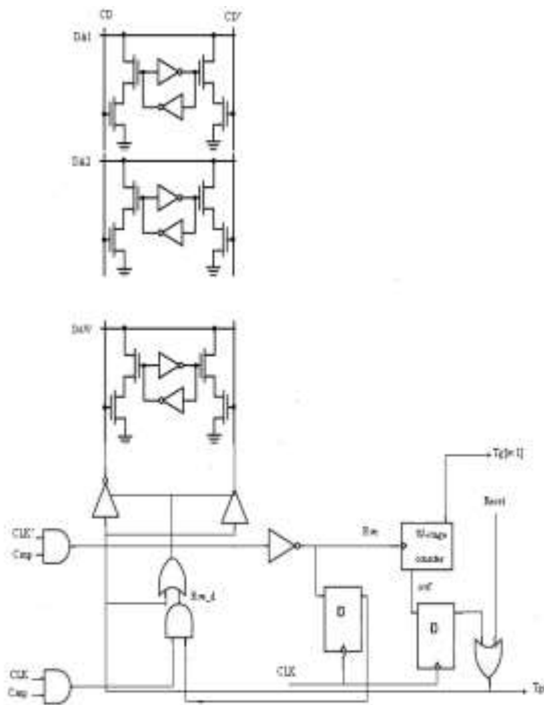


*Fig 4: Proposed logic module*

The operation of the logic module consists of 4 modes of operation:

*1. Reset of the module:*

At the beginning of the operation, the module is reset through the external reset signal. When the reset signal is enabled, the tge signal is enabled and all the outputs of the decoder are enabled. Hence, DA1, DA2…DA*W* are one; furthermore, the CD' signal is enabled; therefore, a one is written to the right hand side of the cam cells and a zero value to the left hand side of the cam cells.

*2. Hit of vector:*

During normal mode, the normal input vectors are given to the inputs of the CUT. The normal inputs are also driven to the CBU as follows: the *w* low-order inputs are driven to the inputs of the decoder and the *k* high-order inputs are driven to the inputs of the comparator. When a vector that belongs to the current window reaches the CUT's input, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (CLK' and Cmp are enabled) the addressed cell is read; because the read value is zero, the *w*-stage counter is triggered through the NOT gate which outputs the Response verifier enable (Rve) signal. During the second half of the clock cycle, the left flip-flop: the one whose clock input is inverted enables the AND gate whose other input is CLK and Cmp, and enables the buffers to write the value one to the addressed cell.

3. *Vector That Belongs in the Current Window Reaches the CUT Inputs but not for the First Time:*

If the cell corresponding to the incoming vector contains a one, the Rve signal is not enabled during the first half of the clock cycle; hence, the w-stage counter is not triggered and the AND gate is not enabled during the second half of the clock cycle.

*4. Tge operation:*

When all the cell values are equal to one, then the value of the *w*-stage counter is all one. Hence, the Rve signal is enabled which enables the counter overflow (ovf) signal; in the next clock cycle the Tge signal is enabled through the unit flip-flop delay and all the cells are set to zero because all the outputs of the decoder of are enabled. When switching from normal to test mode, the *w*-stage counter is reset.

## SIMULATION RESULTS

In this section the simulations results of proposed input vector monitoring concurrent BIST architecture using CAM cell are presented. The designs are coded in VERILOG language and simulated using ModelSim PE Student Edition 10.3c. A codeword of size 15 is chosen here for designing. The front end design of the architecture, synthesis and comparison are done using Xilinx ISE Design Suite14.1i.

The simulation result of the proposed scheme is shown in the figure 5. The proposed technique operates as same as that of the existing technique[4] ,except that in the Concurrent BIST Unit(CBU)block ,SRAM cell is replaced by a Content Addressable Memory(CAM)cell of the logic module to reduce the area overhead and concurrent test latency(CTL),the time required to complete the testing during normal operation. Also the modified decoder block is removed because for the CAM cell the data is its input.

*Fig 5: Simulation Result of the Proposed Scheme*

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

The synthesis report for the proposed technique is shown in the figure 6.

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| **Total Number Slice Registers** | 13 | 1,920 | 1% | |
| Number used as Flip Flops | 2 | | | |
| Number used as Latches | 11 | | | |
| Number of 4 input LUTs | 20 | 1,920 | 1% | |
| **Logic Distribution** | | | | |
| Number of occupied Slices | 13 | 960 | 1% | |
| Number of Slices containing only related logic | 13 | 13 | 100% | |
| Number of Slices containing unrelated logic | 0 | 13 | 0% | |
| **Total Number of 4 input LUTs** | 20 | 1,920 | 1% | |
| Number of bonded IOBs | 10 | 66 | 15% | |
| **Total equivalent gate count for design** | 191 | | | |
| Additional JTAG gate count for IOBs | 480 | | | |

*Fig 6: Area Report for the Proposed System*

Table 1 and 2 shows the comparison results of area overhead and concurrent test latency (CTL) for the existing and proposed techniques.

***Table 1 Comparison of Equivalent Gate Count***

| Techniques | Total Equivalent Gate Count |
|---|---|
| Existing system | 298 |
| Proposed system | 191 |

***Table 2 Comparison of Concurrent Test Latency***

| Techniques | Concurrent Test Latency(CTL) |
|---|---|
| Existing system | 3270 ns |
| Proposed system | 3150ns |

The proposed method is been compared with the existing method with respect to hardware overhead and concurrent test latency .The existing design requires 3270 ns to complete the test during normal operation and its hardware overhead is 298 gates . The proposed design just requires 3150ns to complete the test and its hardware overhead is 191 gates.

Therefore, from the above two tables there is a reduction in the testing time completion when compared to existing system.

## CONCLUSION

BIST schemes constitute an attractive solution to the problem of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can circumvent problems appearing in offline BIST techniques.The evaluation criteria for this class of schemes are the hardware overhead and the CTL, i.e., the time required for the test to complete, while the circuit operates normally. In this proposed technique, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of CAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

## REFERENCES


1. E. J. McCluskey, "Built-in self-test techniques," IEEE Design Test Computers., volume. 2, no. 2, pp. 21–28, Apr. 1985.
2. I. Voyiatzis, A. Paschalis, D. Gizopoulos, N. Kranitis, and C.Halatsis, "A concurrent BIST architecture based on a self testing RAM," IEEE Transaction on. Rel., volume. 54, no. 1, pp. 69–78,Mar. 2005.
3. I. Voyiatzis and C. Halatsis, "A low-cost concurrent BIST scheme for increased dependability," IEEE Transactions on. Dependable Secure Computers., volume. 2, no. 2, pp. 150–156, Apr. 2005.
4. Ioannis Voyiatzis and Costas Efstathiou, "Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells ",IEEE Transactions on Very Large Scale Integration (vlsi) systems, vol. 22, no. 7, July 2014.
5. K. K. Saluja, R. Sharma, and C. R. Kime, "A concurrent testing technique for digital circuits," IEEE Transactions on. Computer Aided Design Integrated Circuits and Systems., volume w. 7, no. 12, pp. 1250–1260, Dec. 1988.
6. R. Sharma and K. K. Saluja, "Theory, analysis and implementation of an on-line BIST technique," VLSI Design, volume. 1, no. 1, pp. 9–22, 1993.
7. K. K. Saluja, R. Sharma, and C. R. Kime, "Concurrent comparative built-in testing of digital circuits," Department of Electronics

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

and Computer Engineering., University of Wisconsin, Madison, WI, USA, Tech. Rep. ECE-8711,1986.

8. I. Voyiatzis, T. Haniotakis, C. Efstathiou, and H. Antonopoulou, "A concurrent BIST architecture based on monitoring square windows," in Proc.5th Int. Conf. DTIS, Mar. 2010, pp. 1–6.
9. M. A. Kochte, C. Zoellin, and H.-J. Wunderlich, "Concurrent self-test with partially specified patterns for low test latency and overhead," in Proceedings on 14th European Test Symposium., May 2009, pp. 53–58.
10. S. Almukhaizim and Y. Makris, "Concurrent error detection methods for asynchronous burst mode machines," IEEE Trans. Comput., vol. 56, no. 6, pp. 785–798, Jun. 2007.
11. S. Almukhaizim, P. Drineas, and Y. Makris, "Entropy-driven parity tree selection for low-cost concurrent error detection," IEEE Transactions on Computer Aided Design Integrated Circuits and Systems., volume. 25, no. 8, pp. 1547–1554,Aug. 2006
12. J. Rajski and J. Tyszer, "Test responses compaction in accumulators with rotate carry adders," IEEE Transactions on Computer Aided Design Integrated. Circuits and Systems. Volume. 12, no. 4, pp. 531–539, Apr. 1993.
13. I. Voyiatzis, "On reducing aliasing in accumulator-based compaction," in Proc. Int. Conf. DTIS, Mar. 2008, pp. 1–12.
14. L. R. Huang, J. Y. Jou, and S. Y. Kuo, "Gauss-elimination based generation of multiple seed-polynomial pairs for LFSR," IEEETrans. Comput. Aided Design Integr. Circuits Syst., vol. 16, no. 9,pp. 1015–1024, Sep. 1997.
15. Y. Zorian and A. Ivanov, "An effective BIST scheme for ROM's,"IEEE Trans. Comput., vol. 41, no. 5, pp. 646–653, May 1992.